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Protocol

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Biotemplated precise assembly approach toward ultra-scaled high-performance electronics

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Supplementary Information

for

Bio-templated precise assembly approach towards ultra-scaled high-performance electronics

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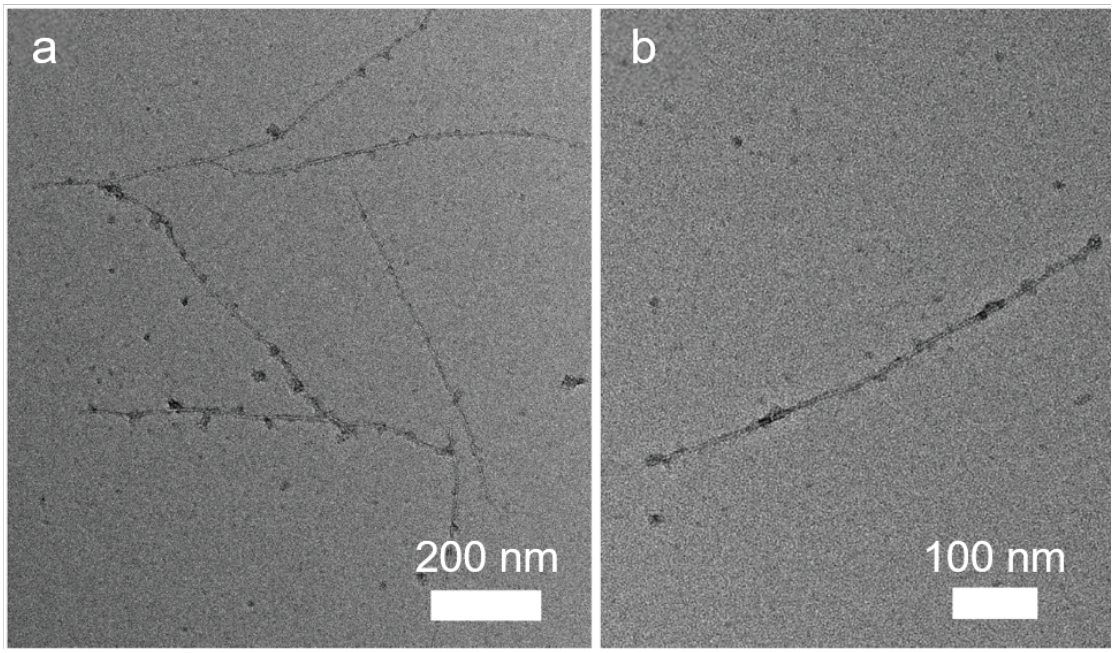
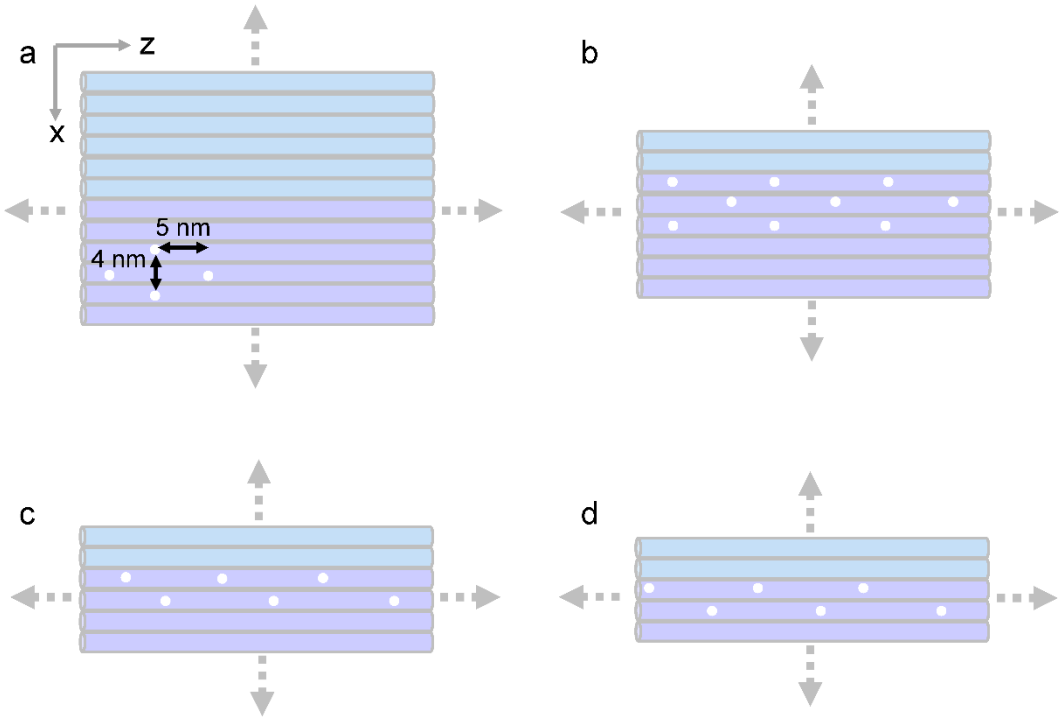
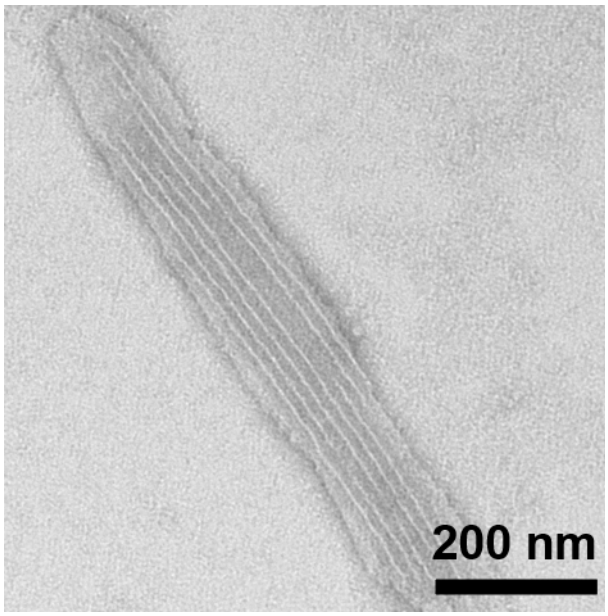


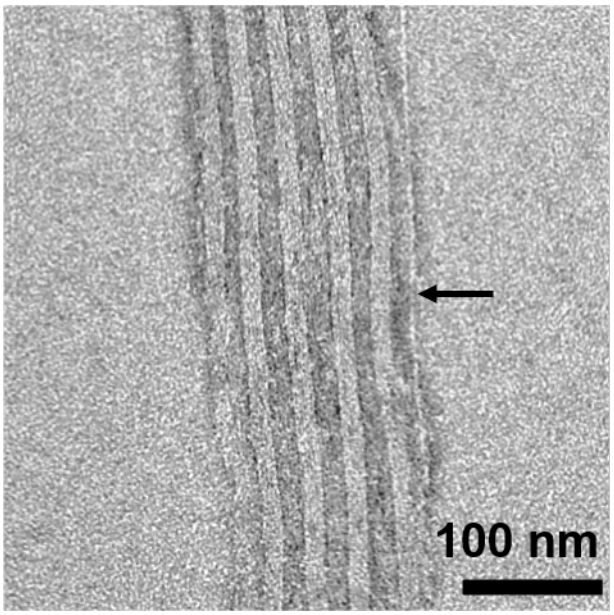
Supplementary Figure 1. A typical TEM images of ssDNA-wrapped CNTs, (a) zoomed-out and (b) zoomed-in images after staining. TEM images are adapted with from ref.[38].



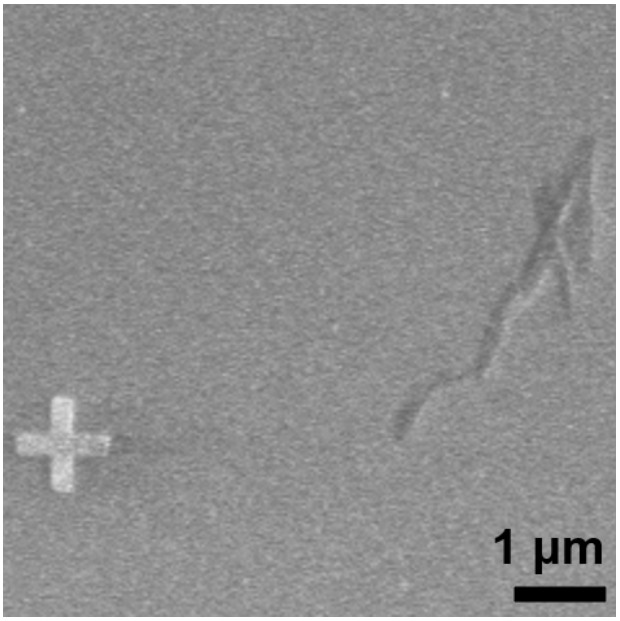
Supplementary Figure 2. Schematic of different DNA handles designs within DNA nano-trenches. The blue- and purple-colored bundles show a repeating unit of sidewall and bottom layer of nano-trenches. White dots represent the location of DNA handles within 25.3-nm (a), 16.8-nm (b), 12.7-nm (c), and 10.6-nm (d) periodicity nano-trenches. Gray arrows denote the assembly directions of DNA template.



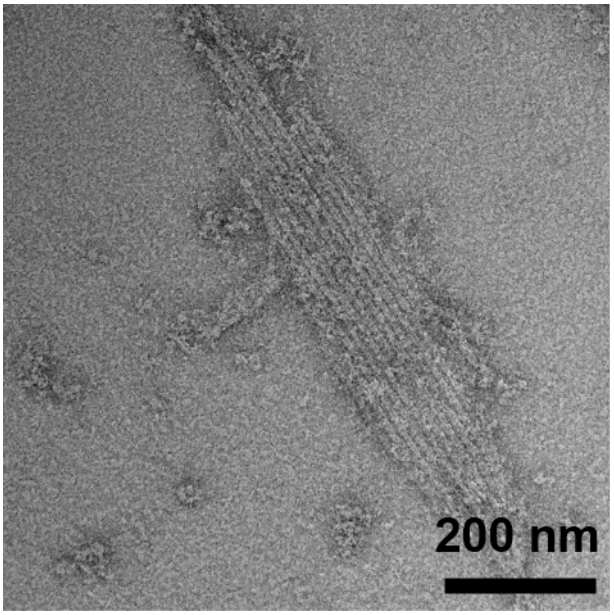
Supplementary Figure 3. A typical TEM image showing the incomplete DNA sidewalls on the DNA templates due to the missing of DNA strands during the mixing.



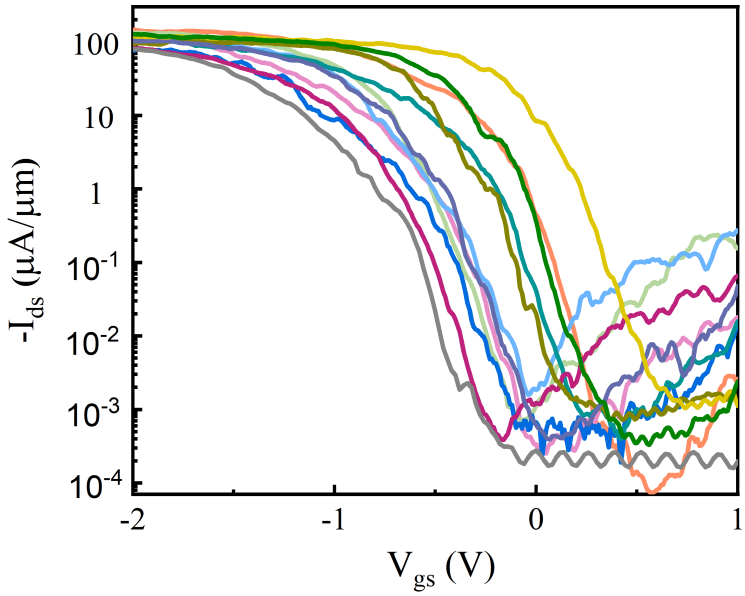
Supplementary Figure 4. A typical TEM image showing low assembled yield of CNT arrays within DNA template. Black arrow denotes the location of CNT.



Supplementary Figure 5. A typical SEM image showing the aggregation of DNA templates on the silicon substrate.

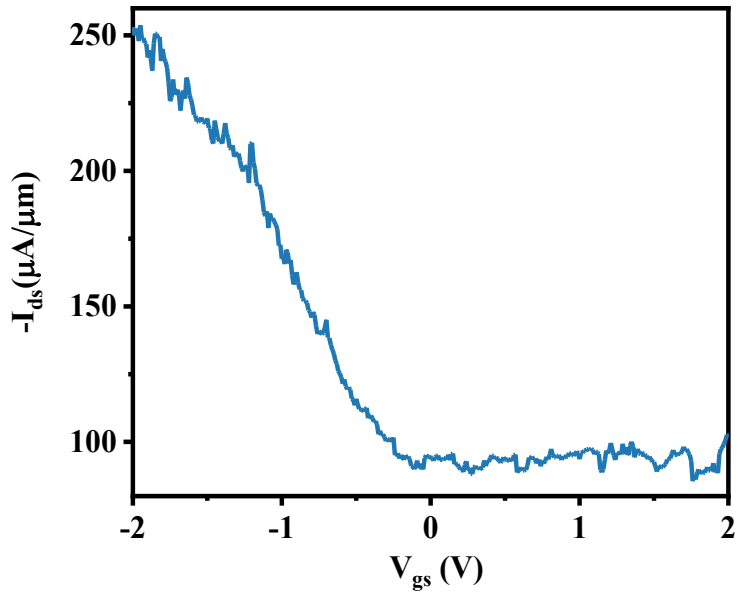


Supplementary Figure 6. A typical TME image shows salt-covered CNT-DNA template structure.



Supplementary Figure 7. 12 multi-channel CNT FETs showing on/off ratio larger than three orders of magnitudes at V_{ds}= -0.5 V.

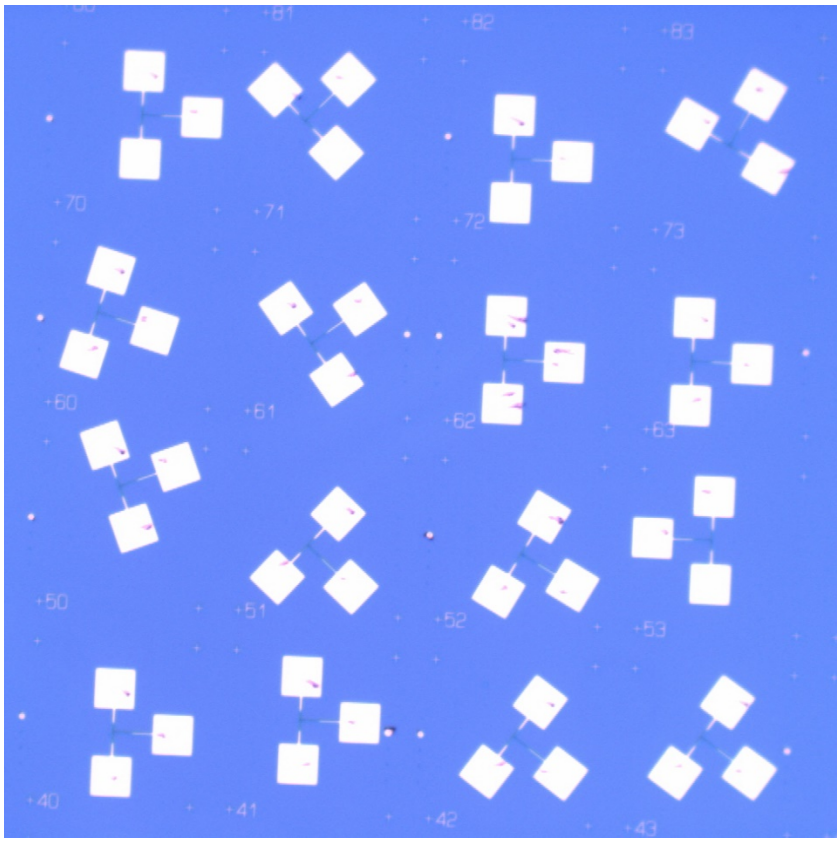
Statistics of all the 12 multi-channel FETs exhibit I_{on} of 80 to 154 μA/μm (at V_{ds} of -0.5 V and V_{gs} of -2 V). The subthreshold swing is about 107 ± 14 mV/dec. The field effect mobility is ranging from 262 ~ 473 $cm^2 \cdot V^{-1} \cdot S^{-1}$.



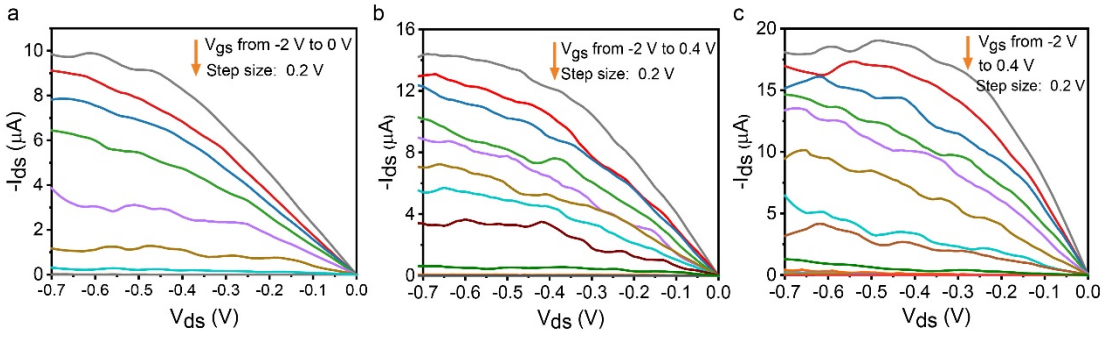
Supplementary Figure 8. A typical I_{ds}-V_{gs} curve for the multichannel CNT FET containing metallic CNTs inside. The on/off ratio is less than one order of magnitude at V_{ds}= -0.5V.

In a single batch, 12 of 17 total devices showed gate modulation exceeding 10^3. The rest of 5 devices contained at least one metallic CNT within the channel, displaying the I_{on}/I_{off} ratio less than one order of magnitude (supplementary figure 8). The metallic CNT can be separated from semiconducting CNTs. Different methods have been reported to improve the semiconductor purity

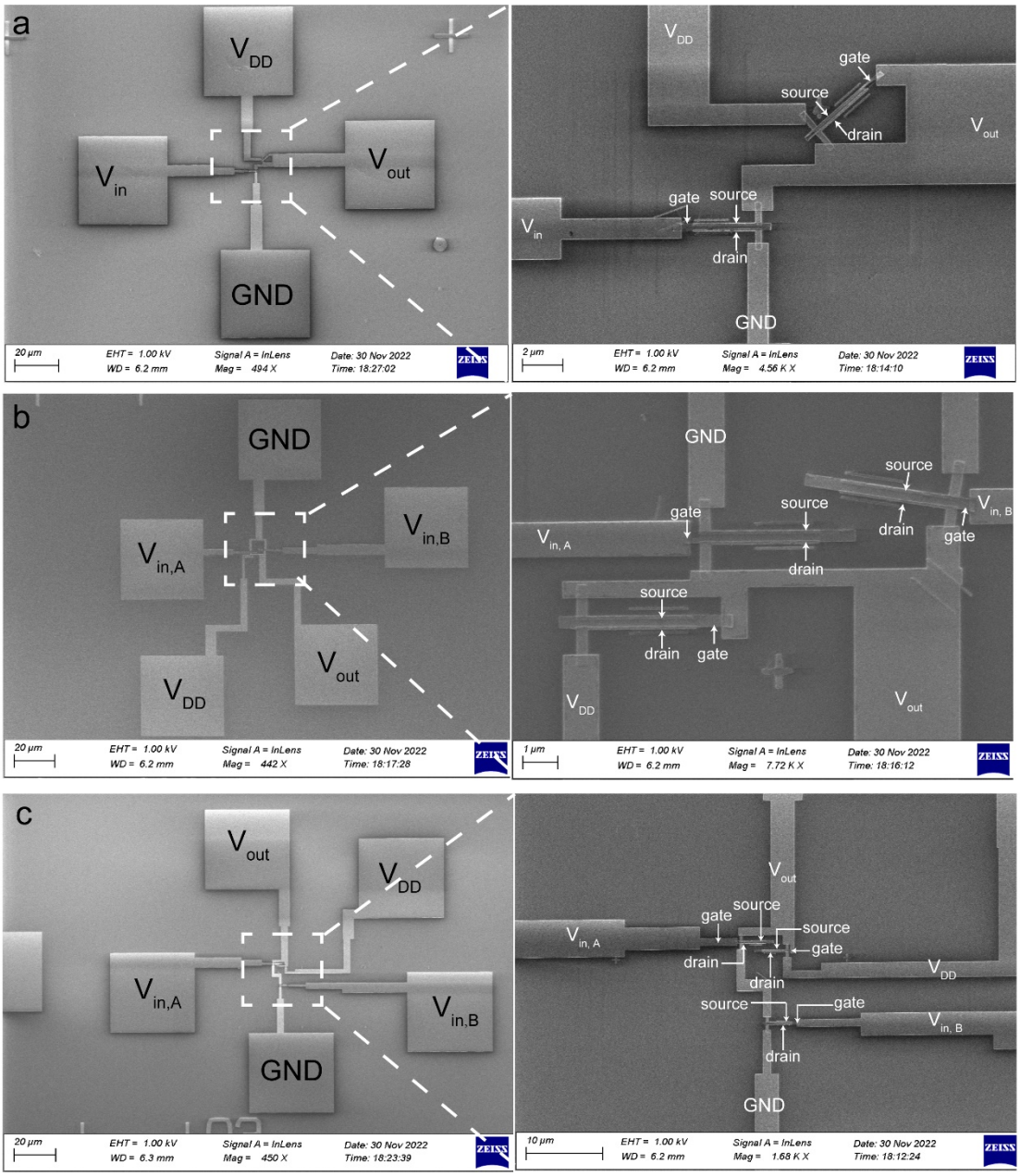
of solution-based or CVD-grown semiconductor CNT, which can achieve semiconductor purity exceeding 99.9999%.



Supplementary Figure 9. Optical image showing volume fabricated single-channel CNT FETs with different channel lengths.



Supplementary Figure 10. Output characteristic of single-channel CNT FETs with 200 nm channel length at V_{gs} ranging from -2 V to 0 V at a step size of 0.2 V (a); with 75 nm channel length at V_{gs} ranging from -2 V to 0.4 V at a step size of 0.2 V (b); with 50 nm channel length at V_{gs} ranging from -2 V to 0.4 V at a step size of 0.2 V (c).



Supplementary Figure 11. Representative SEM images showing logic gates from single-channel CNT transistors, including (a) inverter, (b) NAND, and (c) NOR. Left images are the zoomed-out image with different pad functions denoted in the image. Right images are the zoomed-in images, the white circles showing the zoomed-in areas in the left panels.